The Intel® 840 Chipset

New Bandwidth Horizons for Servers and Workstations

Introduction

The benefits of increased processor speeds are highlighted in a number of venues. However, advances in key platform subsystems including I/O, memory, graphics and the interface to the processor itself must also keep pace to minimize bottlenecks throughout the entire system. The chipset is a key component in supporting advanced platform interfaces and improving system throughput.

Historically, chipset designs have focused on uni-processor rather than multi-processor systems. The Intel® 840 chipset was specifically designed to meet the needs of high-performance multi-processor systems. The 840 chipset, together with the latest Intel® Pentium® III processor or Intel Pentium III Xeon™ processor, provides new levels of performance, scalability, and end-user productivity.

The Intel 840 chipset delivers significantly increased system bandwidth over its predecessors and desktop siblings in the key areas of memory, I/O and graphics subsystems. This increased bandwidth allows outstanding performance in multi-processor systems, while also enabling the use of high-bandwidth peripherals.

The 840 chipset incorporates two new key technologies which are especially relevant for workstation users, namely AGP 4x graphics support and Direct Rambus* memory. These technologies increase capabilities in the critical areas of graphics and memory over traditional solutions. The 840 chipset supports two RDRAM* channels to provide the highest memory bandwidth in any high-volume IA platform. AGP 4x, often implemented as AGP Pro in 840 chipset-based platform designs, provides 1GB/sec of graphics bandwidth and has extended electrical and thermal envelopes to provide support for best-of-class advanced graphics cards.

Intel has six major initiatives reflected in the 840 chipset. The first one listed here, Intel® Scalable Bandwidth Technology, sees its first embodiment with the Intel 840 chipset architecture; the other five are common across the current Intel® 800 series chipset product family, and reflect the benefits of commonality throughout multiple product platforms.

Intel Scalable Bandwidth Technology introduces a full set of system interfaces that use the latest serialization, clocking and signaling techniques to deliver outstanding bandwidth-per-pin across all interfaces. Further, these interfaces can be scaled by increasing clock frequency or width, to deliver higher bandwidth without compromising the system architecture or demanding major software changes. The 840 chipset has two such examples in its architecture. The first is the implementation of dual-channel Direct RDRAM* based memory channels, delivering 3.2GB/sec of bandwidth into main memory. The second is the optional high-speed 533MB/sec hub interface that delivers sufficient bandwidth to directly support PCI-64 interface. Furthermore, the AGP Port, in conjunction with AGP Pro, provides a scalable graphics solution, supporting AGP 1x, 2x and 4x interfaces and graphics card power requirements from 25 up to 110 watts—all on a single interface. With Intel Scalable Bandwidth Technology, multiple platforms with targeted capabilities may be designed using the 840 chipset.

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Stable platforms allow IT managers to deploy large numbers of systems that run an identical software image. The 840 chipset's use of Intel® Hub Architecture allows Intel to enhance and update components of the chipset without necessarily forcing new system images into the installed base. Coupled with stabilized device drivers, the platform will deliver an extended deployment life cycle, allowing IT managers to deploy systems with a life cycle period of greater than 12 months.

Constant computing reflects the ability of a platform to perform multiple functions in the background without compromising foreground performance. These background tasks can perform continuous virus checks, compress and decompress network traffic for more effective use of bandwidth, scan the hard drive for problem areas and automatically repair defects. The 840 chipset architecture, along with Direct RDRAM memory, can support multiple simultaneous memory access threads without penalty. The Intel® Hub Architecture allows isochronicity for I/O devices, to guarantee quality of service (QoS) for time sensitive applications such as audio or video.

Rich content delivery allows users and content providers to interact more effectively over the constrained bandwidth of the Internet. Initially, compression and decompression technologies will be the primary features, but 3D object modeling will increasingly deliver dramatically reduced bandwidth and increased image quality. In the 840 chipset, the introduction of RDRAM memory and AGP 4x graphics support provide the local processing bandwidth to deliver outstanding 3D graphics.

Platform security provides the hardware foundation for software security technologies that will minimize concerns about privacy and security in electronic transactions. These advances will greatly reduce the risks for all electronic commerce participants, including banks, buyers, sellers, corporations and individuals. The PC and the Internet will provide the medium for greatly accelerated business processes, ultimately with lower risk than paper-based systems. The firmware hub in the 800 series of chipsets, including the 840 chipset, implements an Intel® random number generator (RNG), providing the first hardware-based security enhancement for the Intel® platform.

Manageability is enhanced by the Alert-on-LAN* (AOL) feature, which allows the computer to report its status to the network controller, even if the computer is incapable of booting due to hardware or software error. The 840 chipset has watchdog timers that can detect and restart a hung system without user intervention. This chipset also provides improved sleep and wake features, supporting the Instant-On specification, for improved power management and better acceptance of the always-on PC.

The Intel 840 Chipset and System Manufacturers

The 840 chipset, introduced on October 25, 1999, provides the highest Intel 2-way performance platform for the year 2000 and beyond. System manufacturers will find that its advanced, high-bandwidth buses and advanced feature set lead to performance-leading designs that can extract the full performance of the Intel Pentium III processor or Intel Pentium III Xeon processor. The combination of the 1 GB/s AGP 4x interface, 3.2GB/sec of main memory bandwidth, 533MB/sec bandwidth of the PCI-64 interface, and advanced SIMD and streaming instructions of the Pentium III processor and Pentium III Xeon processor, allows 840 chipset-based platforms to deliver today's top-of-the-line performance for multi-processor systems. Furthermore, the commonality of subsystems that the 840 chipset shares with other members of the 800 chipset family will substantially reduce design, development and qualification time. These characteristics will allow system manufacturers to deliver tremendous value based on price/performance, and offer users new opportunities for productivity gains.

The 840 Chipset and Business Users

The 840 chipset is designed for high-end platforms, intended for workstation and volume server applications. Although not designed for general business use, its family similarities with the other 800 series of chipsets render the product easier to manage in a corporate IT environment. For employees involved in such tasks as computer-aided design/analysis, still or motion video editing, data analysis/visualization, or simulation, the 840 chipset will offer a significant boost in performance over other platforms. Furthermore, the I/O capabilities of the 840 chipset are especially supportive of user collaboration over high-speed networks. Therefore, 840 chipset-based platforms should be deployed to users that require such computing-intensive capabilities.

In a server environment, the high memory bandwidth, multi-processor capabilities, support for PCI-64 interface, and validation with an optional RAID controller companion chip qualify the 840 chipset to support large, fast storage arrays.

The 840 Chipset and Windows* 2000

Windows* 2000 is a major advance in operating system technology, bringing a new measure of stability, security, flexibility and functionality to the PC. The 840 chipset, in conjunction with the Intel Pentium III processor or

Pentium III Xeon processor, will deliver the platform performance to support this new operating system, its advanced features, and its derivatives, providing greater investment protection for IT managers. Windows 2000 incorporates improved multi-processor support, a feature that will be of high value when combined with the increased efficiency of the 840 chipset in a multi-processor environment. Furthermore, the double-width (32-bit) RDRAM bank and deep internal FIFOs provide outstanding support for multitasking or multithreaded software. Intel expects the 840 chipset to become a natural combination with Windows 2000 for both server and workstation applications.

The 840 Chipset and Workstation Users

The bandwidth of the 840 chipset, coupled with the option to support dual Pentium III Xeon processors, will allow 840 chipset-based systems to compete with the most advanced workstations and provide clear leadership in price/performance measures. The introduction of PCI-64 interface to the platform will give Intel-based workstations standard access to the most advanced and sophisticated peripheral cards available. These systems will also be priced competitively with 1998's high-end desktops, bringing the benefits of multi-processor capability to a new class of user.

The 840 Chipset and Consumers

The 840 chipset was not designed for the mainstream consumer market. These users, invariably supported by a single processor, will most likely obtain the greatest value from the Intel® 820 chipset in conjunction with a high-performance consumer AGP 4x card. However, performance technologies pioneered in the 840 chipset will no doubt migrate their way into future generations of Intel® chipset products targeted for consumer desktops.

The 840 Chipset: Overview and Siblings

The 840 chipset represents Intel's platform initiative for workstation and server products that will ship throughout 2000, with expected shipments well into 2001. It is designed to be the platform of choice for the Pentium III processor and Pentium III Xeon processor architecture when used in a multi-processor environment, providing full support for the bandwidth and instruction processing capabilities of these configurations. It is the highest performance part of a family of chipsets that will support all single and dual processor computing market needs in 2000. This family currently includes: the Intel® 810E chipset, for low-cost systems; the 820 chipset, for mainstream performance systems; and the 840 chipset, for workstation and volume server applications. Table 1 shows the relationship between these three chipsets. Note that all chipsets share the same firmware hub and I/O controller hub, an important factor in delivering consistent and stable platforms.

The 840 chipset embodies a plethora of technology advances, enhancing management features over previous chipsets, increasing interface bandwidths, delivering performance headroom for future processors, and implementing the first platform hardware security features. The chipset also embodies a new interconnect architecture (Intel® Hub Architecture), transitioning the PCI bus to a peripheral role in favor of the use of high-speed low pin count buses. This new architecture doubles or quadruples aggregate bandwidth in every critical area over that of its predecessor, the Intel® 440GX AGPset. It also supports the 133MHz processor system bus (PSB) introduced on the Pentium III processor. The Intel Pentium III processor and Pentium III Xeon processor have an enhanced bus interface and are capable of fully exploiting this bandwidth.

Table 1. Intel's new platform chipsets

Chipset	Intel® 810E Chipset	Intel® 820 Chipset	Intel® 840 Chipset
System cost	Low	Mainstream	Premium
Defining feature	Integrated graphics	Mainstream performance	Bandwidth and scalability
Maximum processors	1	2	2
Memory	100MHz SDRAM	1 RDRAM channel SDRAM with MTH	2 RDRAM channels (PC600/800) SDRAM with MRH-S
PCI	32 bit	32 bit	32-bit and 64-bit
Target processor(s)	Intel® Celeron™ processor	Pentium III processor (1 or 2)	Intel® Pentium® III Xeon™ processor (1 or 2)
	Intel Pentium III processor		Pentium III processor (1 or 2)

Technology Background

To understand the 840 chipset, it is helpful to understand the two major challenges facing system designers today: electrical integrity and system bandwidth. This section gives a background on each of these issues and sets the stage for understanding the advanced bus technologies implemented in the 840 chipset.

Electrical Design Challenges

An electrical pulse traveling down a wire is a complex phenomenon. James Clerk Maxwell derived a set of equations in the late 19th century that so effectively modeled and predicted the behavior of electrical signals that he was able to predict the existence of radio waves. These equations exposed the essential duality of electrical signals: some travel inside the conductor, some travel outside of it. Depending on the physical dimensions of the conductor and the rate of change of the signals, more or less energy will be distributed outside of the conductor. If this energy transfers to another circuit, or is not properly controlled inside its own circuit, signal integrity can be lost and reliability is compromised.

As this containment problem scales with higher frequencies, higher currents, complex layouts and more conductors, the solutions are clear: lower voltages and hence lower currents, fewer conductors, simpler circuit paths, and advanced design and simulation practices. In practice, fewer conductors bring a double benefit: Less energy can escape and the circuit paths become considerably simpler. The 840 chipset incorporates five such highly controlled buses: the Processor System Bus (PSB); the Direct Rambus memory interface, AGP 4x graphics support, and the two hub interfaces (8-bit and 16-bit). The LPC interconnect bus, while not in the same bandwidth category of these other buses, benefits from pin count reduction techniques. These buses can be easily scaled by advancing their clock frequencies, while their physical simplicity reduces the design challenge. In the future, new high-speed serial buses such as System I/O and USB 2.0 will displace other parallel buses in the system, further reducing complexity and enhancing system integrity. Table 2 shows the performance of the buses in the 840 chipset and, where applicable, significant electrical integrity features.

Table 2. Intel® 840 Chipset Bus performance and integrity features

	Bandwidth	Effective transfer rate	Type	Feature
Processor System Bus	1GB/sec	133MHz	Multidrop	GTL+
Direct Rambus	3.2GB/sec	800MHz	Controlled bus	Low voltage
AGP4x	1GB/sec	133MHz	Point-to-point	Low voltage
Hub Interface (8-bit)	266MB/sec	266MHz	Point-to-point	Active matching
Hub Interface (16-bit)	533MB/sec	266MHz	Point-to-point	Active matching
LPC	4MB/sec	33MHz	Multidrop	

Electrical Integrity: Summary

In summary, the 840 chipset incorporates the following advances to contain the inherent challenges that result from Maxwell's equations:

- Hub Interface 8 (HI8), a reduced pin count high-integrity bus for system interconnect
- Hub Interface 16 (HI16), a double-width version of HI8
- Dual Direct Rambus for memory interconnect
- Advanced cabling for ATA/66 hard drive interconnect
- A new 1.5V signal level for AGP4x

These enhancements increase reliability and performance while lowering system cost. Designers are cautioned, however, that these buses are unforgiving of layout deficiencies and must be handled with respect. The Intel 840 chipset application note provides full layout design details for these new buses.

The Bandwidth Challenge

As processor technology advances, both clock rates and work done per clock increase. These advances in processor performance demand increased performance through the entire system if the full processor performance is to be realized. Table 3 shows how the 840 chipset outperforms its new desktop sibling, the 820 chipset, and its predecessor, the Intel® 440GX chipset.

Note the tremendous bandwidth provided through the use of dual Direct Rambus channels. The system has sufficient memory bandwidth to support full transfer rates on all of its buses to and from memory without incurring a performance penalty. The Hub Interface 16, connected to the memory controller hub, provides the 533MB/sec needed to support the PCI-64 bus interface, four times the bandwidth of the traditional 32-bit PCI bus.

Table 3. System Bandwidth Comparison: Intel 840, Intel 820, and Intel 440GX Chipsets

	Intel 840® Chipset	Intel® 820 Chipset	Intel® 440GX AGPset
PSB	Intel® Pentium® III processor or Pentium III Xeon™ processor (133 MHz PSB) 1,024 MB/s	Intel Pentium III processor (133 MHz PSB) 1,024 MB/s	Intel® Pentium II processor (66–100 MHz PSB) 512–728 (MB/s)
Graphics	AGP4x 1,066 MB/s	AGP4x 1,066 MB/s	AGP 2x 533 MB/s
Memory	PC800 DRDAM 3,200 MB/s	PC800 DRDRAM 1,600 MB/s	100 MHz SDRAM 800 MB/s
Bridge Bus A	Hub Interface 8 266 MB/s	Hub Interface 266 MB/s	PCI 133 MB/s
Bridge Bus B	Hub Interface 16 533 MB/s	NONE	NONE
HDD	ATA/66 66 MB/s	ATA/66 66 MB/s	ATA/33 33 MB/s

The 840 Chipset Architecture

Intel's new 840 chipset consists of three core components, and three optional components to scale Intel 840 chipset-based systems. The core components are: a Memory Controller Hub (MCH, 82840); an I/O Controller Hub (ICH, 82801); and a Firmware Hub (FWH, 82802). The optional devices are: the PCI-64 hub (82806); the RDRAM-based memory repeater hub (MRH-R, 82803) and the SDRAM-based memory repeater hub (MRH-S, 82804). LPC Super I/O device is used to provide legacy I/O. The chipset takes its name from the memory controller hub, but shares a common firmware hub and I/O controller hub with its contemporaries (Table 1). This commonality of system components guarantees that the new chipsets share identical software for features and enhancements implemented in these peripheral devices and reduces development, implementation and support costs. The hub architecture with its narrow, high-speed buses also saves pins: the 840 memory controller is packaged in a 544 pin mini BGA package and has a total of 785 pins between its two major components, compared to 816 on the 440GX chipset. This reduction in pin count brings with it a reduction in manufacturing cost and increased reliability, while system capabilities far exceed that of the 440GX chipset.

Reduced Pin Count Buses

The 840 chipset incorporates four reduced pin count buses that increase data transfer rates through the use of narrower buses but higher-speed, scalable clocks. The first of these is the Direct Rambus interface, a new memory interface that adds up to 1.6GB/sec of memory bandwidth in a 33-pin bus for each memory channel; the 840 chipset has two such channels, for a total of 3.2GB/sec of available bandwidth.

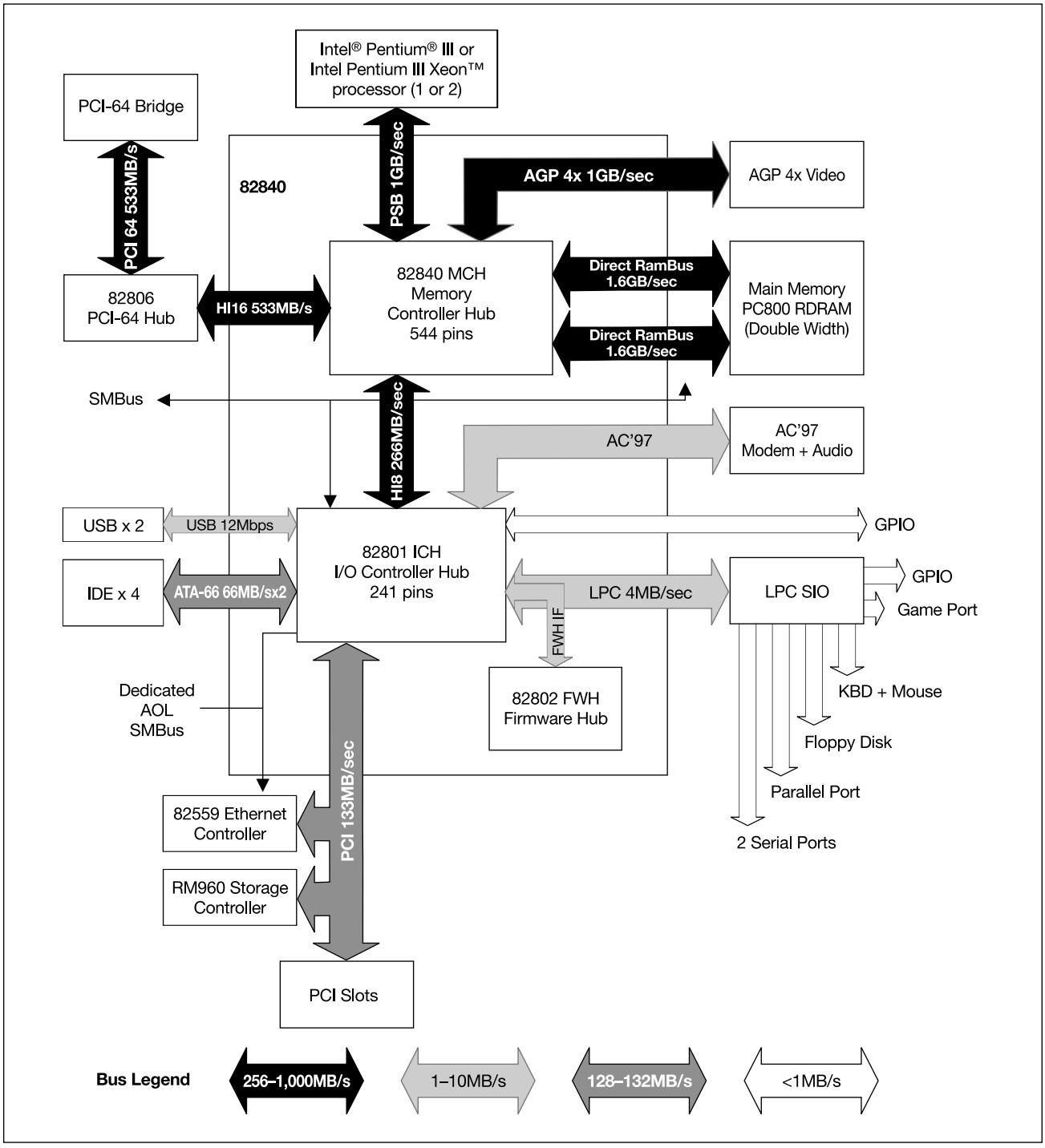
The second is the hub interface, which replaces the PCI bus as the internal interconnect between the core logic and the internal system peripherals. It delivers 266MB/sec in a one-pin bus. The hub interface is a point-to-point bus with a monitoring signal line to closely match the signal characteristics to the circuit board layout. It uses eight data lines, two lines for a differential strobe, three lines for protocol control and two lines for signal integrity. There is an optional parity signal for applications that require it, but the bus is designed for totally reliable data transfer. The strobe signal clocks at up to 133MHz/sec and transfers data at 266MB/sec through the use of both clock edges. The PCI bus is now relegated to a peripheral interface in the I/O controller hub and is removed from the bandwidth-critical core of the system.

The third interface is the hub interface 16, which doubles the number of data and strobe pins in HI8 to deliver 533MB/sec of bandwidth directly to the PCI-64 bus controller. It is otherwise identical to HI8. Use of the HI8 and HI16 demonstrate the modular and scalable architecture upon which Intel will continue to build.

The final interface is the LPC bus, which provides the interface to a controller that supports traditional ISA peripherals including serial, parallel, game and floppy ports, through a seven-pin interface (four data, typically three control). The LPC interface also provides the electrical connection for the firmware hub interface, which supports the BIOS flash memory and the RNG function.

Figure 1 shows the 840 chipset architecture in its entirety.

Figure 1. The Intel® 840 Chipset System Architecture



Intel® Hub Architecture

Previous generation chipsets used the PCI bus to connect the north bridge and south bridge of the chipset. However, with Intel 800 series chipsets, the PCI bus has been moved to simply become an extension of the I/O Controller Hub, and Intel® Hub Architecture is used to connect the Memory Controller Hub to the I/O Controller Hub and PCI-64 Controller Hub.

The Intel® Hub Architecture partitions the system into three major components. It is distinguished by its use of a very high bandwidth (266MB/sec and 533MB/sec), reduced pin count interface called the hub interface. The hub interfaces on the 840 chipset provide increased bandwidth of 266MB/sec and 533MB/sec with just 16 pins and 25 pins, respectively. Its bandwidth and

architecture allows the chipset to deal effectively with isochronous data without the bottlenecks associated with the PCI protocols. This bandwidth is achieved through the use of very high clock rates, differential signaling on the strobe line, a reference voltage signal that guarantees reliable switching, and a compensation signal that allows the chip to match its buffer characteristics to those of the printed circuit board. The bus is source-synchronous—the clock and data are driven at the source, guaranteeing synchronous arrival. The combination of source-synchronous clocking and the voltage and matching signals guarantees electrical integrity, but a parity option is available for those applications that require signal checking throughout the system such as high-integrity servers. The interface signals and their functions are shown in Table 4.

Table 4. Hub Interface 8 pin Count

Function	Pins	Comment
Data bits	8	
Strobe	2	Differential signal supports 266MHz transfer rate
Control	2	
Parity (Optional)	1	Requires support from the 840 MCH
Trace matching	1	Matches signals to circuit board
Hubref	1	Signal voltage reference

The Hub Interface 16 doubles up the data and control bits for a total width of 25 signals, over which the interface can transfer 533 MB/sec to support 64-bit /66 MHz PCI.

The memory controller hub incorporates the memory controller, the hub interface 8, the hub interface 16, the AGP 4x interface, and processor system bus interface. The I/O controller hub incorporates a hub interface, the PCI interface, the USB controller, the ATA/66 controller, the AC'97 controller, and LPC interfaces for the firmware hub and legacy I/O. The firmware hub incorporates the BIOS flash memory and the random number generator.

Traditional PC I/O functions including legacy serial and parallel I/O, the floppy interface, and the game port are supported by a Super I/O part with an LPC bus interface. The 840 chipset is not validated to support ISA peripherals.

The 82840 Memory Controller Hub

The MCH is the heart of the system, linking all of the major components—processor, graphics, memory and I/O—together through high-performance buses. It has an aggregate bandwidth of 6.1GB/sec, and its multipath concurrent internal design permits peak transfer rates of 2.9GB/sec.

Multi-processor Support

The 840 MCH supports two Intel Pentium III processors or Intel Pentium III Xeon processors at a PSB speed of 133MHz.

Accelerated Graphics Port 4X (AGP 4x)

The AGP architecture was developed to address the ever-increasing bandwidth needs of graphics accelerators. The initial implementation, AGP 2x, delivered twice the bandwidth of PCI. Consequently, the first generation AGP bus was connected directly to the memory controller to avoid overload of the PCI bus.

AGP 4x graphics support provides more bandwidth for advanced graphics systems, allowing transfer rates in excess of 1 GB/s. AGP 4x brings with it the electrical challenges described previously in this document. The solution is a change in the interface voltage to 1.5V, down from the 3.3V used in AGP 2x. To provide compatibility with AGP 2x components, the 840 MCH incorporates intelligent buffer technology, which senses and selects the correct signaling voltage for the interface.

AGP Pro, an extension of AGP specification, provides more power and cooling capability to the graphics subsystem. This support system enhancement permits the design of graphics cards with powerful processors and large memory capacities. Signals and the protocols remain identical to those in the AGP specification, so systems designed with AGP Pro are backward compatible to traditional AGP implementations. AGP Pro supports the transfer rates supplied by the AGP 2x or AGP 4x specification and power requirements up to 110 Watts.

The additional graphics bandwidth provided by AGP 4x demands a corresponding increase in main memory bandwidth, delivered by the use of the 3.2GB/sec Direct Rambus interface. In conjunction with the Intel Pentium III processor or Pentium III Xeon processor with SSE and AGP Pro, the 840 chipset opens up new opportunities for advanced graphics systems.

Direct Rambus DRAM (DRDRAM)

Dynamic memory has a long history, pioneered by Intel in the 1970s. Even then, memory capacity advanced at such a rate that it soon became clear that direct addressing of the memory capacity of a single device demanded more pins than necessary, driving up chip and system packaging costs. The architecture of DRAM is such that it is sensible to provide the address in two successive words—the row address and the column address—reducing the pin count of the package and the complexity of the circuit board in exchange for a trivial increase in controller cost. Therefore, DRAMs have historically received two address inputs and returned one data output.

In the late 1980s, microprocessors began to outpace the transfer rate of DRAMs, so the slight variations on the architecture evolved. First came fast page mode, in which the memory controller uses just one row address, but provides multiple column addresses to extract the data from memory. Next came EDO, in which the DRAM accepts the next column address before it provides the data from the previous request. This overlapping allows a doubling in the DRAM transfer rate. Then came synchronous DRAM, which provides an address then extracts successive memory locations through the application of a clock, eliminating the circuit noise and timing overhead of providing incremental addresses to the memory (the memory incorporates a counter that allows it to generate its own column addresses). Over this period, system designers widened the memory data path to 64 bits to allow the transfer of eight bytes at a time, yielding a peak transfer rate of 800MB/sec with 100MHz synchronous DRAM.

Further advances in memory speed are possible. Designers are showing 133MHz SDRAM systems and also the ability to use both edges of the clock to further double transfer speeds. However, Maxwell's equations erect a fundamental barrier at these speeds, demanding expensive circuit board designs to transfer 64 bits of data through connectors and traces without compromising reliability. Furthermore, the need for increased bandwidth demands wider buses, but increasing memory densities force memory arrays that become too large. These are some of the fundamental physical reasons why SDRAM will yield to Direct Rambus in high-performance systems.

The Direct Rambus interface represents a new approach to memory interfacing. The 12 address bits, 4 control bits and 64 data bits of a conventional memory array are replaced by a single 16-bit bidirectional bus, clocked on both edges of a high-speed 400MHz clock and providing maximum data transfer rates of 1.6GB/sec per device. The bus carries commands to the memory, and transfers data in both directions in response to these commands. The lower pin count of the Rambus interface allows designers to accept a more challenging electrical design task in exchange for relatively simple, easily-manufactured designs that can deliver high data rates with a minimum component count. The low pin count allows channels to be easily added to a controller, providing a practical method to scale bandwidth for several generations of chipset. This is manifested in the 840 chipset, which uses two memory channels.

Initial Direct Rambus memory modules will be available with transfer rates of 600, 700 and 800MHz and will be designated as PC600, PC700 and PC800 memory respectively. The 840 supports PC600 and PC800 to enable system and memory manufacturers to better optimize performance, yield and cost.

Multiple Hub Interfaces

The 840 chipset uses the 8-bit 266MB/sec hub interface (HI8) to connect to the standard 800 series I/O subsystem. It also introduces a 16-bit variant of HI8, capable of transferring data at 533MB/sec. This interface provides the necessary bandwidth to support PCI-64, and has the potential to support other advanced high-speed buses in the future. HI16 is a derivative of HI8, and shares the same electrical and design characteristics. It adds eight data and two strobe signals to transfer 533MB/sec across a total of 25 signal pins.

The 840 Chipset Memory Architecture

The 840 chipset memory architecture incorporates a double-banked Direct Rambus system, delivering 3.2GB/sec of aggregate peak bandwidth. The interface is designed to be used as 32 bits wide, requiring that the two channels be populated symmetrically. This approach doubles up the width of the independent banks in the RDRAM devices, providing a wider memory line size that lends itself to multithreaded applications. The memory architecture also includes two optional components, the 82803 RDRAM memory repeater hub and the 82804 SDRAM memory repeater hub to aid in the implementation of large memory subsystems that can accommodate either DRDRAM or PC100 SDRAM, respectively.

The 82803 RDRAM-based Memory Repeater Hub (MRH-R)

The RDRAM memory repeater hub accepts one Direct Rambus channel at its input, and delivers two Direct Rambus channels at its output. This device allows for the development of larger memory subsystems while keeping the electrical parameters within the constraints of the Direct Rambus specification. Each MRH-R supports up to 64 RDRAM components.

The 82804 SDRAM-based Memory Repeater Hub (MRH-S)

In server applications, memory capacity is typically even more important than memory performance. Large memory subsystems can be divided into many banks, allowing the main memory to be interleaved. This approach delivers higher performance in multithreaded and multi-processing environments. These large memory systems can offer bandwidth equal to that of RDRAM,

although implemented with SDRAM. On the 840 chipset, it is necessary to place 2 MRH-S on each of the two DRDRAM controllers to allow memory interleaving, and extract the full 3.2 GB/s of bandwidth. With a single MRH-S on each memory channel, 1.6 GB/s of memory bandwidth is available, twice that of the 440GX chipset.

The MRH-S incorporates a DRDRAM controller on the system side, and an SDRAM controller on the memory side. This component allows systems to be implemented with either DRAM architecture.

The MRH-S can be placed on the motherboard or built onto a vertical memory expansion card, allowing arrays of SDRAM to be populated. With a memory expansion card-based design, a user can switch from an SDRAM-based system to an RDRAM-based system, simply by changing the memory card and rebooting the computer. Systems must be built using just one type of DRAM. The 82804 is not compatible with RDRAM in the same system.

The 82802 Firmware Hub

The firmware hub incorporates system features that have no external interface. In the 82802, this category includes the flash memory and the Intel random number generator (RNG). It has its own unique protocol, but shares the LPC bus interface pins to connect to the I/O controller hub. This multiplexing approach reduces system pin count and complexity.

Flash Memory

The firmware hub provides the boot flash memory for the system, and is available in both 4Mb (512KB) and 8Mb (1MB) configurations. The larger size provides for integrated BIOS designs and offers the opportunity to perform sophisticated preboot management, diagnostic and security functions.

The Intel® Random Number Generator (RNG)

One of the great challenges to any secure system is the proper generation of keys. For example, an encryption system that uses a 40-bit key (the largest key generally permitted under export control laws) can be cracked in a matter of hours on a modern PC. By contrast, the 56-bit key used in DES takes decades of effort to crack on a single PC, and a 128-bit symmetric key is beyond the bounds of all known or projected cracking technology advances.

However, the security of a 128-bit cipher can be completely negated by the selection of an overly simple key. For example, English text has an effective key length of about 1.4 bits per character. Therefore, a 20-character passphrase is equivalent to a 28-bit key and easily cracked by a personal computer. It is extremely difficult for a human to produce sufficient randomness to realize the strength of a 128-bit key. Furthermore, software RNGs suffer the same problem. Algorithms that use the time of day, the date, and any other system variables available to them still fall far, far short of even generating a secure 56-bit key.

Therefore, the 840 chipset firmware hub incorporates a hardware RNG. The device uses thermal noise in a semiconductor junction to produce random circuit transitions. These transitions are aggregated and checked for true randomness, then assembled into a random key of any desired length. A software driver can use this hardware to deliver truly random bitstreams to security applications, guaranteeing that security will not be compromised because of the selection of a weak key and that users can have truly private conversations.

The 82801AA I/O Controller Hub (ICH)

The 82801AA ICH performs the functions previously embodied in the south bridge. However, the higher bandwidth of the hub interface allows the hub to offer dramatically increased performance. This is particularly important in the areas of the ATA/66 interface, which would otherwise consume all traditional PCI bus bandwidth, and the AC’97 and USB interfaces, which require controlled response times and throughput to deliver uninterrupted audio and modem connections, and other features, to the user.

Alert on LAN* (AOL)

Current manageability solutions provide great insights into the state of a functional PC, but do not address the case of a PC that is unable to boot. The 840 chipset allows even a non-booting machine to report basic status to a network management host. It achieves this through its AOL feature, which implements processor-independent state machines that can report status data to the network administrator even if the processor is incapacitated. This data is reported over a dedicated unidirectional SMBus interface, a low-speed serial bus for power management and low-level control and reporting functions. Future chipsets will use a bidirectional interface to support AOL 2.0, conferring on the PC the ability to power up in response to a remote command. The 840 chipset requires an Intel® 82559 network controller (or compatible product) to provide the AOL service. It is expected that other manufacturers will incorporate the technology into their controllers. The ICH and the 82559 incorporate simple state machine devices capable of reporting system hard-

ware status to a predefined host address with no processor intervention. The information includes relevant hardware management bits stored in the 840 chipset:

- Chassis intrusion
- Processor not present
- Custom messages
- Watchdog timer
- Thermal event monitor

Chassis Intrusion

By means of an optional sensor—mechanical, or optical, or both—connected to the chassis, the ICH can detect and remember the opening of the system cover. This function operates even when the system is disconnected from the power supply. The function is valuable to system administrators as it announces that the system might have been subjected to tampering. Such tampering would include the installation of unauthorized or unapproved peripherals, or removal or substitution of the processor, memory or hard drive.

Processor Not Present

The ICH monitors processor activity and can detect when the processor stops or fails to fetch its first instruction. The AOL interface can report this status to the network administrator.

Custom Messages

The ICH incorporates a message register that is reported to the AOL interface during the boot process. The BIOS can set bits in the register to report boot status across the network.

Watchdog Timer

The watchdog timer restarts the processor in the event of a system crash. This event can be reported to the network administrator, alerting the possibility of system problems.

Thermal Event Monitor

The ICH supports a single thermal event monitor signal. If this signal trips, it can report to the administrator. Often, system failures are caused by thermal problems inside the machine or in its environment. This feature can aid in identifying such issues. An example is an air-conditioning system that fails on a hot day, causing unidentifiable system failures.

ATA/66

The high-end hard drives available in 1999 achieve a data transfer rate from the media to the head of approximately 350Mb/sec, or (after error correction and adjustment for track-to-track seek time) about 33MB/sec. This transfer rate represents the maximum sustained rate that the drive can deliver to the system, although its burst rate may be higher because of on-board caches. The ATA/33 interface can handle this data rate, but recent advances require an improved interface to avoid throttling system performance due to a limited data transfer rate to the hard drive. Furthermore, ATA/33 already added error detection and correction to the interface, greatly reducing the risk of data corruption at higher transfer rates.

ATA/66 is a natural extension to the existing high-speed ATA/33 hard disk drive interface. Transferring two bytes of data per clock edge, four bytes per clock, it is capable of maximum sustained burst transfer rates of 66MB/sec. Achieving these high-speed data rates is a challenge to the electrical design of the system, a problem solved by the addition of 40 ground wires to the existing 40-wire IDE cable. Therefore, ATA/66 systems use 80-wire cable with 40-pin connectors. Substituting these cables with regular IDE cables will potentially result in degraded performance because of the excessive errors that a regular IDE cable could induce. Users and manufacturers should be aware of this problem.

A Performance Driver Opportunity

Note that the ATA/66 implementation in the 800 series I/O controller hub consists of two independent, identical controllers located on the internal PCI bus. Each controller is capable of sustained data transfer at the maximum rate of the interface, which peaks at 66MB/sec. The use of the Intel® Hub Architecture and RDRAM memory provides sufficient bandwidth for both controllers transferring data at maximum rate into the main memory without compromising other system activity. This was not possible on previous generation platforms, as the combined bandwidth of the hard disk controllers saturates a standard PCI bus. This new headroom presents the opportunity to develop a striping driver for dual IDE hard drives, delivering peak transfer rates of 133MB/sec. This combined transfer rate, coupled with the new generation of 40GB and higher capacity hard drives, presents the opportunity for low-cost desktop platforms that deliver disk performance suitable for workstation applications without incurring the cost of a SCSI storage subsystem.

AC’97

AC’97 is a new audio interface designed to improve cost, quality and stability of the PC audio subsystem. The ICH incorporates the digital component of the AC’97 interface.

The key electrical feature of the AC’97 architecture is the divorce of the analog and digital subsystems. This separation dramatically reduces digital noise in the

analog subsystem and enables the use of low-cost, high-quality CODECs. All of the analog data is passed over a five-wire serial bus that uses time division multiplexing. There are three control channels and up to nine 20-bit audio/modem slots available in each direction at a sampling frequency of up to 48KHz. Each slot represents one high-quality mono audio or modem channel. The ICH implements two audio input channels, two audio output channels, a mono microphone channel and a bidirectional modem channel for a total of seven slots.

This arrangement provides two significant advantages. First, the only digital signals in the area of the part are the five serial interface lines (data in, data out, sync., a 12.88MHz clock and reset). Therefore, there is much less digital noise to deal with and the system can deliver a high-fidelity 90dB signal-to-noise ratio. Secondly, the simple interface allows nine audio channels to be managed across just five pins. This capacity allows the CODEC to address most conceivable audio configurations.

The audio modem riser (AMR) feature takes advantage of the low pin count to enable manufacturers to implement the modem, and possibly the audio as well, on an inexpensive riser card. The AMR approach allows the designer considerable flexibility in the implementation of an internal modem to accommodate international regulatory standards, without affecting the audio subsystem.

PCI Bus Interface

The 32-bit PCI bus is supported in the ICH. Unlike previous chipset designs, the PCI bus is no longer central to the system and is not used in the internal datapaths. Although PCI has served the PC architecture well, its bandwidth is no longer sufficient to support the high performance of the PC system core. However, many peripheral devices are available on PCI and it will continue to be the bus of choice for many peripherals and traditional card-based expansion. In the 840 chipset architecture, both 64-bit and 32-bit PCI buses are available for supporting network interfaces.

Legacy I/O and USB

The traditional dual serial ports, parallel port, game port, and keyboard and mouse ports are all supported in the super I/O controller chip. In the 840 chipset architecture, this chip interfaces via the LPC bus, rather than the traditional ISA bus. The reduced pin count of the LPC bus enables the controller to have more pins allocated to interface functions, or to be housed in a lower-cost package.

SMBus and GPIO

There are two additional components worthy of mention. The SMBus interface made its desktop debut in the Intel® 430TX chipset. In the 840 chipset, it is used to extract RDRAM control information; a second, dedicated SMBus channel passes AOL information to the Ethernet controller. Original equipment manufacturers (OEMs) can use the SMBus to add other features to the platform. Power control and platform management features are targets for this interface.

The 840 chipset provides two sets of GPIO, one from the ICH and one (optional) from the LPC super I/O device. These signals provide a handful of general-purpose control lines that can be used by the OEM to differentiate its products.

The 82806 PCI-64 Interface Hub (P64H)

The 82806 P64H provides support for the PCI-64 interface. PCI-64, through the use of 64 data bits and 66MHz PCI clock, delivers a peak transfer rate of 533 MB/sec, and is the fastest general-purpose pluggable interface available today. To support this bandwidth, it connects to the MCH through the high-speed 16-bit hub interface (HI16).

The 80960RN Raid Controller

This optional device connects to the standard PCI bus, and provides fully-qualified integrated RAID support to the 840 chipset-based platform. It is based on the high-performance Intel® 80960 RISC processor, and reflects Intel's I_2O initiative. The option provides high-performance, redundant disk support within the confines of a desktop or small server platform at a lower cost than a typical add-in card solution. The controller can also support single-drive configurations, and is an attractive base feature for systems built around the 840 chipset.

Conclusion

The Intel 840 chipset provides a large number of system improvements. Capabilities such as AGP 4x, 64-bit PCI, ATA/66, and the 133 MHz PSB support advanced platform components. These performance-oriented subsystems are balanced by a high bandwidth memory interface to maximize system throughput. The 840 chipset enables a highly scalable design, with flexibility for graphics, I/O, and memory. The use of narrow, high-speed interfaces improve system reliability and manufacturability. These benefits, combined with the latest Pentium III processor or Pentium III Xeon processor provide end users a highly capable platform for the needs of today and tomorrow.

For more information, visit the Intel Web site at: developer.intel.com

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